REMARKS

Claim 9 has been amended. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made." No claims have been added or cancelled. Accordingly, claims 1-71 are pending.

Claims 9 stands objected to due to a typographical error. Claim 9 has been amended as suggested by the Examiner. Accordingly, the object to claim 9 should be withdrawn.

Applicant's representative appreciates the allowance of claims 13-24 and 35-71, and the indication of allowable subject matter in claims 5-9, 11-12, 26-27, and 29-34.

Claims 1-4, 10, 25, and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Morgan (U.S. Patent No. 5,883,827). This rejection is respectfully traversed.

The present invention is directed an apparatus and method for writing data ina programmable conductor memory. In such memories, a programmable conductor element is used to store the state of a memory cell. More specifically, the programmable conductor element can be set to high or low bi-stable resistive states. In traditional programmable conductor memory system, a high current driver is utilized to provide a writing voltage to force a programmable conductor element from a high resistive state to a low resistive state. As noted on page 3, such an architecture is not power efficient because the write driver continues to supply the high current write voltage even after programmable conductor element switches to a low resistive state.

The present invention takes advantage of the capacitance associated with the bit lines to eliminate the need for a high current write driver. More specifically, a first predetermined voltage is applied to a first terminal of a programmable conductor memory element and a bit line is charged to a second voltage. A capacitance associated with the bit

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line (e.g., parasitic capacitance, or if parasitic capacitance is insufficient, parasitic capacitance plus a coupled capacitor) holds the bit line potential at the second voltage. An access transistor controls whether the bit line is coupled to a second terminal of the programmable conductor element The second voltage is chosen from a set of two predetermined voltages such that when the bit line is coupled to the programmable conductor element through the access transistor, a first of the two predetermined voltages will force the programmable conductor memory element to a first bi-stable state while a second of two predetermined voltages will force the programmable conductor memory element to a second bi-stable state. The apparatus and method of the invention is more power efficient because a high current write driver is no longer required. Accordingly, claim 1 recites "precharging a conductor to a first voltage value" and "coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element." Claim 25 recites "precharging a bit line to a first voltage," "applying a second voltage to a first terminal of a chalcogenide memory element," and "connecting a second terminal of said chalcogenide memory element to said bit line to ... write a predetermined resistance state into said memory element."

Morgan discloses a method and apparatus for reading and writing data to a programmable conductor memory system. The Office Action alleges that the only difference between Morgan and the present invention is that Morgan fails to teach or suggest the step of setting a bit line to a predetermined voltage before writing the programmable conductor memory element. The Office Action further suggests that since precharging is a well known operation in the memory arts, it would have been obvious to incorporate the step of setting a bit line to a predetermined voltage before a write operation in order "to provide sufficient potential for the bit line." It is respectfully submitted that the motivation suggested by the Office Acton is defective for at least the following reasons: the present invention operates by generating one of two potential differences between the first and second terminals of a programmable conductor memory element by setting the first terminal to a predetermined voltage and setting the second terminal to one of two other predetermined voltages. While the operation of setting a bit line to a predetermined

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voltage, i.e., precharging, is a known in some types of memories for specific reasons it is not known to use it in the context of the programmable conductor memory. There is no teaching or suggestion in Morgan which supports the Office Action's assertion that this operation could be used to write the state of a programmable conductor memory element. It is respectfully submitted that only the present specification discloses precharging bit lines to as part of a procedure to write the state of a programmable conductor memory element, and therefore the Office Action has used impermissible hindsight in constructing the motivation for the rejection.

Claims 1 and 25 each recite precharging a bit line to a first voltage and applying the first voltage and a second voltage to a programmable conductor (or chalcogenide) memory element. This discussed above, this feature is not taught or suggested by the prior art of record. Accordingly, claims 1 and 25 are believed to be allowable over the prior art of record. Claims 2-12 and 26-34 depend from claims 1 and 25, respectively, and are also believed to be allowable for these reasons and because the combination recited in the claims are not taught by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Please rewrite claim 9 as follows:

9. A method as in claim 3 wherein said first voltage is [us] ground and said second voltage is at or approximately at Vdd/2.